CLAIMS

We claim:

1. In a magnetoresistive memory device, a method comprising applying a bias current to a word line of the memory device to impose a bias field on a magnetoresistive element for centering a hysteresis loop of the magnetoresistive element.

2. The method of Claim 1, further comprising:

making a determination that that the device switched from a first state to a second state while applying the bias current; and

in response to the determination, triggering a rewrite to restore the memory device to the first state.

3. The method of Claim 1, wherein the step of applying a bias current occurs during a read sequence of the memory device, and wherein the hysteresis loop is a read hysteresis loop.

4. The method of Claim 3, further comprising holding a binary state of the memory device constant while applying the bias current.

5. The method of Claim 1, wherein the step of applying a bias current occurs during a write sequence of the memory device, and wherein the hysteresis loop is a write hysteresis loop.

6. The method of Claim 1, wherein the memory device is a giant magnetoresistive memory device.

7. The method of Claim 1, wherein the memory device is a magnetic tunneling junction device.

8. The method of Claim 1, wherein the bias current is within the approximate range of 5 mA to 40 mA.

9. A magnetoresistive device comprising:

a magnetoresistive element;

a word line arranged near the magnetoresistive element for switching a state of the magnetoresistive element and for applying a bias field to the magnetoresistive element;

a bias driver electrically connected to the word line for applying a bias current to the word line;

a write driver electrically connected to the word line for applying a switching current to the word line.

10. The magnetoresistive device of Claim 9, wherein the bias driver is configured to apply the bias current during a write cycle of the write driver, wherein the magnitude and direction of the bias current is configured to substantially limit a write hysteresis loop bias of the magnetoresistive element.

11. The magnetoresistive device of Claim 9, wherein the bias driver is configured to apply the bias current during a read cycle of the magnetoresistive device, wherein the magnitude and direction of the bias current is configured to substantially limit a read hysteresis loop bias of the magnetoresistive element.

12. The magnetoresistive device of Claim 9, wherein the magnetoresistive element is a giant magnetoresistive element.

13. The magnetoresistive device of Claim 9, wherein the magnetoresistive element is a magnetic tunneling junction.

14. The magnetoresistive device of Claim 9, wherein the magnetoresistive element is an anisotropic magnetoresistive element.

15. The magnetoresistive device of Claim 9, wherein the magnetoresistive element comprises:

a nonmagnetic nonconducting barrier layer sandwiched between two ferromagnetic conducting layers.

16. The magnetoresistive device of Claim 9, wherein the magnetoresistive element comprises:

a nonmagnetic conducting layer sandwiched between a first ferromagnetic layer and a second ferromagnetic layer, wherein the coercivity of the first layer is greater than the coercivity of the second layer.

17. The magnetoresistive device of Claim 9, wherein the magnetoresistive element comprises:

an antiferromagnetic layer;

a ferromagnetic pinned layer coupled to the antiferromagnetic layer;

a nonmagnetic conducting layer coupled to the pinned layer; and

a ferromagnetic free layer coupled to the conducting layer.

18. The magnetoresistive device of Claim 9, further comprising:

means for making a determination that the magnetoresistive element switched from a first state to a second state while applying the bias field; and

means for returning the magnetoresistive element to the first state in response to the determination.

19. The magnetoresistive device of Claim 18,

wherein the means for making a determination comprise a data storage medium for storing a pre-biasing state of the magnetoresistive element; and a comparator for comparing the pre-biasing state with a post-biasing state of the magnetoresistive element, and

wherein the means for returning the magnetoresistive element to the first state comprise a rewrite trigger for causing the write driver to deliver a sufficient current to the word line to switch the magnetoresistive element from the second state to the first state.

20. A magnetoresistive device comprising:

a primary magnetoresistive element, wherein the primary magnetoresistive element is configured to switch between a first state with a low zero-field resistance and a second state with a high zero-field resistance when a magnetic field of sufficient strength is applied to the primary magnetoresistive element;

a complementary magnetoresistive element, wherein the complementary magnetoresistive element is configured to switch between a first state with a high zero-field resistance and a second state with a low zero-field resistance when a magnetic field of sufficient strength is applied to the complementary magnetoresistive element;

a primary bit line electrically connected to the primary magnetoresistive element;

a complementary bit line electrically connected to the complementary magnetoresistive element;

a word line electrically isolated from the primary magnetoresistive element and electrically isolated from the complementary magnetoresistive element, and wherein the word line is aligned near the primary magnetoresistive element and near the complementary magnetoresistive element, and wherein a current in the word line causes a magnetic field to be applied to the primary magnetoresistive element and to the complementary magnetoresistive element, and wherein the magnetic field applied to the primary magnetoresistive element is of the same magnitude but opposite sign to the magnetic field applied to the complementary magnetoresistive element;

a bias driver electrically connected to the word line for generating a bias current in the word line; and

a write driver electrically connected to the word line for generating a write current in the word line.

21. The magnetoresistive device of Claim 20, further comprising a summing device for additively combining the bias current and write current, wherein the bias driver and write driver are each electrically connected to the summing device as inputs and the word line is electrically connected to the summing device as an output.

22. The magnetoresistive device of Claim 20, further comprising:

a comparator for determining whether a change occurred to either a state of the primary magnetoresistive element or to a state of the complementary magnetoresistive element after applying the bias current; and

a rewrite trigger for causing the write driver to generate a current sufficient to return the states of the primary and secondary magnetoresistive elements to their pre-biased states.

23. The magnetoresistive device of Claim 20, wherein the bias drive is configured to create a bias current in the word line of sufficient magnitude to substantially center a hysteresis loop of the primary magnetoresistive element and to substantially center a hysteresis loop of the complementary magnetoresistive element.

24. A magnetoresistive memory array comprising:

a plurality of magnetoresistive memory cells arranged in rows and columns;

a plurality of bit lines, wherein each bit line aligned in one row and coupled to each memory cell in the row;

a plurality of word lines, wherein each word line is arranged near a column of memory cells, wherein a current passing through a word line creates a magnetic field acting along an easy axis of each of the memory cells in the column of memory cells;

a write driver for generating a write current, wherein the output of the write driver is electrically connected to one or more of the plurality of word lines; and

a bias driver, wherein the output of the bias driver is electrically connected to one or more of the plurality of word lines, the bias driver being configured generate a bias current that substantially centers a biased hysteresis loop of a selected magnetoresistive memory cell.

25. The array of Claim 24, wherein the write driver is configured to deliver a first current with a first magnitude and a first direction, and the write driver is configured to deliver a second current with a second magnitude and a second direction, wherein the first magnitude is equal to the second magnitude and the first direction is opposite to the second direction.

26. The array of Claim 24, further comprising:

a write line interconnected between the output of the write driver and the output of the bias driver; and

a switch for interconnecting the write line to a selected word line.